Unveiling the Next Generation

in Integrated Circuit Substrate Circuit Formation

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The electronic packaging industry has been crippled by the incremental technology advancement produced by substrate manufacturers over the past decade. While semiconductors and related packaging technologies progress at alarming rates, typically doubling in functionality every couple of years, the substrate portion of the integrated circuit (IC) packaging industry continues to fall farther and farther behind. This has created a significant technology gap, forcing semiconductor manufacturers to compensate their chip design by adding more redistribution layers or, even worse, additional size to the chip itself. Thus, the IC industry is in dire need of a significant change at the substrate level to remove the innovative barrier that exists today and allow chip designers to continue their efforts in reducing size and cost while increasing functionality.

A collaborative effort between Amkor Technology, Unimicron, Anvik, and Atotech has led to a significant breakthrough in substrate manufacturing techniques, allowing both layer and format reduction (thus cost reduction) over currently available state-of-the-art technologies. The tremendous growth and need for a disruptive technology in IC substrates has helped facilitate the implementation of this new method that allows miniaturization of both design features and substrate format. This innovative technology uses laser photoablation techniques, together with specially developed plating processes, to form electrical paths for signal propagation within the dielectric, as opposed to conventional technologies that form signal paths above the dielectric.

This technology provides opportunity for significant gap closure to current needs in the chip packaging industry. The laser-structured approach offers a unique opportunity to simultaneously improve upon traditionally incremental improvements in design as well as optimize electrical performance at the same time by reducing signal paths. Ultimately, this approach addresses critical needs for the coming generations of chip-packaged substrates by not only driving miniaturization in design but also by improving the electrical performance of the package. This article unveils the technology and benefits that the laser-embedded approach provides.

Background

Substrate innovation continues to be paced by known technologies in the substrate manufacturing industry, limiting the ability of manufacturers to close gaps that exist between packaging technology and substrate-based technology. Part of this is due to the reliance on incremental approaches to roadmaps and part to limited development budgets within the substrate industry. Margins at the substrate level have forced manufacturers to focus on business and roadmaps with visible demand rather than invest in future technologies that might offer promise in better gap closure to the packaging industry. Additionally, the incremental approach to technology has been predicated on photolithographic techniques and miniaturization of the through-hole. Although this approach has allowed the steady progression of geometries to just under 20 µm signal width and 100 µm via diameter, the primary issue of space utilization and electrical performance still has not been fully addressed. Even with the full adoption of laser blind vias through coreless concepts, the basic problem remains: how to reduce the footprint of the substrate itself while maintaining or improving upon the electrical performance.

A collaborative effort has brought forth a new method of manufacturing substrates that not only allows the miniaturization of signals to 10 µm and below with padless vias and reduction of layers from current design sets today, but also maintains all electrical requirements of the package.[1] This article discusses an overview of the technology, as well as a portion of the findings and conclusions from the work completed to date jointly between Amkor, Unimicron, Anvik, and Atotech. The intent is to convey the overall benefit of the laser-embedded approach from both a cost and performance perspective, in addition to presenting a preview of the beginning of a new era in substrate manufacturing techniques.

Laser-Embedded Approach

Laser-embedded technology is predicated upon the use of a laser to create recesses within the dielectric material for subsequent signal formation, as opposed to current photolithographic techniques used today where signals are formed on the surface of the dielectric. In general, the intent is to not only create much smaller patterned features as a result but to bypass the yield and cost-sensitive photolithography stages as well. Through work completed to date, this has been accomplished with a number of ablation techniques. In fact, multiple laser choices have been tried and proven effective, including both excimer and UV YAG systems, with each offering uniquely different benefits.

Figure 1 Excimer Ablated Signals

The laser-embedded format allows the formation of recessed signals to below 10 µm (4 µm demonstrated) and the creation of near padless vias to facilitate a reduction in both package size and format. Resolution of designed-in features to ±1 µm, with registration at better than

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2.5 µm, is realized with the laser structuring approach. The registration is a direct result of the simultaneous creation of microvias and the completely recessed signal channels. Because the creation of the vias and signals occur simultaneously, all patterned features are precisely aligned, facilitating the landless microvia structures. Thus, as a result, the laser-embedded approach enables significant layer reduction by availing more routing space on each plane of the substrate.

Critical aspects of this approach also include the ability to manage the ablation process with high panel throughput. This, however, is greatly affected by the laser choice and level of integration employed. In this respect, the laser choice will also have tremendous influence on the subsequent substrate fabrication processes. This is especially true when considering the performance and cost tradeoffs of the ablation process chosen (UV YAG versus Excimer). Equipment cost, throughput, maintenance, and consumables are all varying factors affecting the cost equation of this process. However, as discussed in the following section, the cost equation must be balanced with the performance of the final product.

Laser machine technology is developing rapidly and performance standards only a few years ago were replaced by equipment that will ablate the patterns required in seconds rather than minutes. This improvement is the result of not only advances in the laser sources but also in the software and control systems for the machines.

The Laser Structuring Process

Larger features adversely affect the direct write approaches (UV YAG), as the write time is significantly increased as a result. The direct dependence on ablation area requirements highlights a negative characteristic of the direct write approach because larger feature areas require more ablation time to complete and therefore lower the throughput. If large lands are required for subsequent via connections to top-side layers, the time required to crate these lands could be prohibitive, depending on size. Therefore, careful design consideration should be given when considering pad, ground, and other larger patterns. It is important to note that the laser structured approach allows the creation of traces without the need for lands or pads, thus enabling even UV YAG approaches.

Figure 2 Mass Ablation of the Dielectric Surface Area

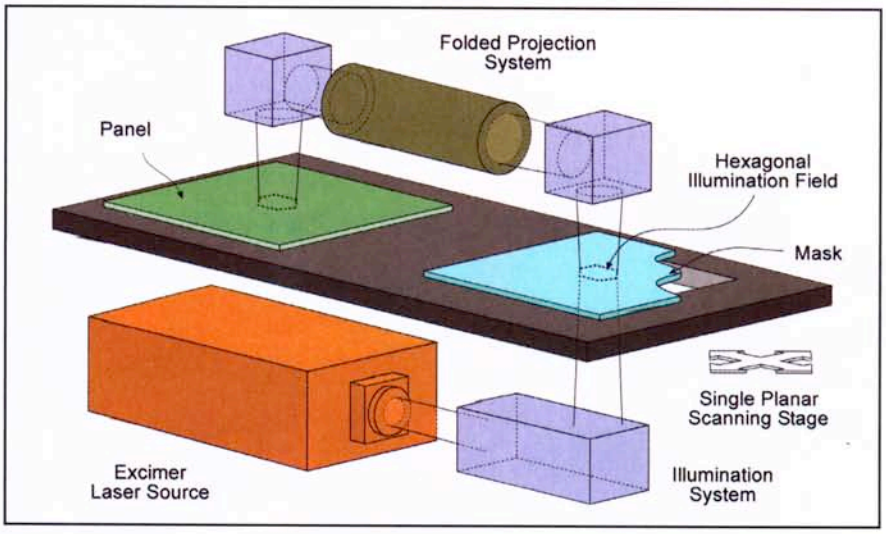

Figure 3 Hexagonal Seamless Scanning Technique

Excimer ablation, on the other hand, allows for better resolution and depth control, as well as higher throughput when the pattern has larger features.[1-4] This can be of significant consequence when considering the creation of lands, ground planes, or other larger features in the patterning process. Figure 1 shows an example of excimer-ablated signals paths at 12 µm line and space. Excimer systems operate at typically 248 or 308 nm wavelengths, providing a more incremental ablation approach to dielectric removal and thus providing high resolution and better depth control. Excimer systems can operate in average power ranges up to 300 W, depending on configuration and projection lens design. Additionally, the mask-based excimer laser projection ablation system provides a unique advantage. It enables mass ablation of the dielectric surface area to create any feature size desired, across a large area, without penalty for increased density (Figure 2).

The Anvik Hexscan 4050 SXE is an excimer laser-based mass photoablation system that uses a unit-magnification projection imaging system to transfer patterns from a photomask onto a substrate. The mask is imaged onto the substrate using a unique hexagonal seamless scanning technique (shown in Figure 3). The Anvik Hexscan 4050 SXE's mask projection technique enables mass ablation of dielectrics over large area substrates without penalty for increased feature density, in direct contrast to UV YAG direct write systems where increased feature density greatly increases the write time and consequently reduces the throughput.

The Anvik Hexscan 4050 SXE (Figure 4) can pattern on a variety of dielectrics with resolutions down to 5 µm with alignment accuracies of ±2.5 µm and very precise depth control of less than 1 µm. It can also carry out photoablation patterning on a variety of thin film metals and ceramics.

Figure 4 Anvik Hexscan 4050 SXE

In the Anvik Hexscan 4050 SXE, the mask and substrate are mounted on the same scanning platform that is capable of moving them synchronously in the x and y directions. The illumination beam is a homogenized hexagonal beam from a KrF

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excimer source, operating at 248 nm, which is capable of providing an output power of up to 300 W. The seamless stitching is achieved by complementary overlap between adjacent hexagonal scans that enables the Anvik Hexscan 4050 SXE to scan across large substrates with uniform exposure dose across the substrate. The system also incorporates Anvik's patented VAST technology that enables tiling a smaller mask over large substrates with the individual tiles aligned with respect to each other with high accuracy, typically of the order of a few microns. The VAST feature allows the use of a smaller mask, significantly reducing the cost of the mask.

The Anvik Hexscan 4050 SXE incorporates a CCD camera-based alignment system that includes pattern recognition software. The relative positions of the mask and substrate are determined by the system software and the information is processed by the system computer and sent to a fine positioning and alignment system (FiPAS), which then imparts a relative x-y-θ correction in the position of the substrate with respect to the mask, bringing

Figure 5 Aramid Non-Woven Fiber With 12 µm Lines and Spaces That Have Been Ablated

the two to the desired alignment. In Figure 5, 12 µm lines and spaces have been ablated in an aramid non-woven fiber.

Figure 6 shows patterned 12 µm lines and spaces (upper right); 60 µm vias located directly between two 110 µm flip chip attach pads (upper left); 420 µm BGA pads (lower left); and 12 µm line and spaces and 110 µm flip chip attach pads (lower right). Because the excimer system is a mass ablation system that uses a projection mask, a multitude of pattern sizes and shapes can be created at the same time.

With the ability of the excimer system to ablate large lands and traces simultaneously, the throughput is also enhanced as compared to the UV YAG systems. This is important for products requiring large lands or ground planes on the same plane as the trace signals.

Figure 6 Patterned 12 µm Lines and Spaces (Lower Right); 60 µm Vias Located Directly Between Two 110 µm Flip Chip Attach Pads (Upper Left); 420 µm BGA Pads (Lower Left); and 12 µm Line and Spaces and 110 µm Flip Chip Attach Pads (Lower Right)

The ability to ablate both at the same time without a throughput penalty is critical, as large features require significant time to create in a direct write system, making the UV YAG system all but impractical in many cases. It is important to note that the line resolution and depth are not compromised when ablating large features adjacent to the signals.

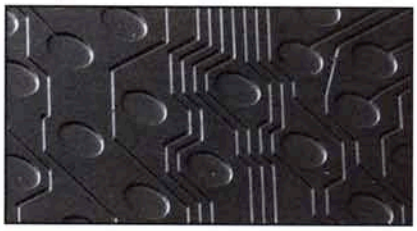

Figure 7 Excimer Ablation of Kapton Dielectric

This is again demonstrated in Figure 7, with 12 µm traces connecting to 250 µm lands in a Kapton dielectric, further demonstrating the precise ability of the excimer projection photoablation system to control depth, registration, and feature size simultaneously.

Depending upon integration techniques of the lens systems, laser power, and optimum know-how, the panel throughput for an excimer system can be 15 panels or more per hour, again depending on the depth of ablation and dielectric choice. Although the excimer system is able to ablate numerous materials while still maintaining the same resolution, precision, and accuracy, the material of choice is preferably a homogenous material (or one with limited silica fillers) to maximize ablation speeds. Figure 8 demonstrates both Aramid and expanded Teflon dielectrics with 12 µm traces and spaces.

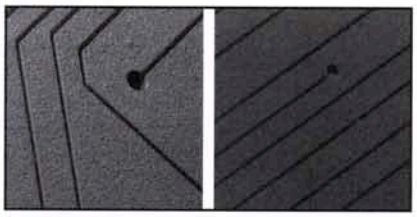

Figure 8 Aramid and Expanded Teflon Dielectrics With 12 µm Traces and Spaces

Unique Attributes of Approach

The laser-embedded approach addresses not only the need to reduce the overall layer count to improve upon both cost and yield concerns, but also the need to improve upon the electrical performance by use of improved routing techniques and reduced signal length. Part of the ability to reduce the number of layers comes directly from the ability to create 10 µm signal traces in conjunction with padless microvias. Due to the ability to ablate the vias and the signal traces simultaneously, the need for registration tolerances has been removed with respect to the formation of each feature or, at the minimum, significantly reduced. With the excimer system, the available registration accuracy is well within 5 µm of fiducials and exact on a feature-to-feature basis.

An additional benefit of the laser-embedded approach is the improvement of circuit adhesion to the dielectric. With standard techniques used today, the copper binds on only one side to the dielectric, creating processing problems and resultant opens or trace cracking under stress. With the laser-embedded approach, the copper

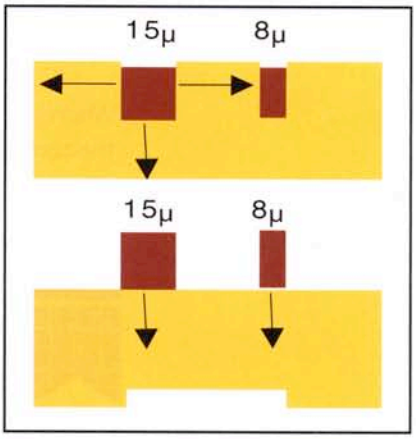

Figure 9 Copper Binds to the Dielectric on Three Sides, Removing Opportunity for Separation of the Circuit From the Dielectric Material

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binds to the dielectric on three sides, thus removing opportunity for separation of the circuit from the dielectric material as a result. This is demonstrated in Figure 9.

It is also important to note that in high-speed applications, the length of interconnect from die pad to I/O can be more important than the dielectric itself. With the reduction in the number of layers and shortened signal paths by means of the laser-embedded techniques, electrical performance is no longer compromised. Additionally, the surface profile of the copper trace also has an effect on the signal integrity at higher speeds. At higher speeds the signal travels more along the surface of the trace rather than in the bulk metal itself. With adhesion of the copper trace to the surface dielectric being of concern in standard processing to assure a high-yield process and a reliable product under stress, a degree of copper surface roughness is required, typically at or near 2 µm. The laser-embedded approach addresses the adhesion to dielectric without having to roughen the copper by binding on three sides, as previously discussed. The issue of adhesion and copper roughness becomes exacerbated in standard semi-additive processing as trace signals continue to reduce to below 15 µm. This issue is removed with the laser-embedded approach.

As the laser-embedded approach allows for much smaller trace signals due to resolution and manufacturing techniques (see Figure 10), it provides the ability to route many more channels on a given plane. This ultimately enables the layer reduction needed for improved electrical performance and cost reduction. It is clear that by reducing the signal width, more signals can be routed between pads.

Figure 10 The Laser-Embedded Approach Allows for Much Smaller Trace Signals Due to Resolution and Manufacturing Techniques

Competitive Solutions

Embossing and very advanced photolithographic techniques that also attempt to create miniaturized features have been tried, or are being contemplated. Embossing requires the use of a tool plate and the ability to release this tool from specialized materials to form recessed features. The embossing technique forms a pattern into the surface of the dielectric by use of a hot press, simultaneously curing the dielectric. Tool cost, lead times, and the need to inventory a large number of tools for each design can make this approach prohibitive. In addition, challenges of tool release from the dielectric as well as dielectric limitations due to embossing affinity have limited this application.

Extremely advanced photolithographic techniques can be found across every substrate supplier's roadmap today. Fabricating smaller features in substrates is driving most IC substrate suppliers to expensive equipment and materials in an attempt to create >15 µm circuits. Steppers, expensive glass tooling, specialized resists, and handling are all required to allow the formation of these circuits. As the circuits go to 12 µm, the challenge becomes even greater with severe yield implications. Additionally, this still does not address the registration issues involved with aligning the vias to pre-formed circuitry.

Transfer solutions provide an additional approach to embedding circuits, using standard photolithographic techniques on advanced resists that have been applied to various carriers. Once the resist has been patterned through the standard (or advanced) photolithographic processing, the patterns are subsequently plated. This image is then laminated (pressed) into the dielectric to embed the circuit. This technology has attributes, but it also has drawbacks. Primarily, it has registration limitations within the transfer process. While registration tolerance to 40 µm is achievable, tolerance to >20 µm still requires significant development. To generate features >15 µm will also require very advanced photolithographic techniques and materials.

Conclusion

Flip chip substrate technology involves the most advanced set of materials and design rules used for substrates in the industry today. Increasing IC functionality continues to drive the addition of layers and, subsequently, cost. Material costs can be as high as 60 to 80 percent of the total flip chip package cost. Layer counts as high as 16 layers are found for advanced application specific integrated circuits. In fact, the addition of layers is continuing to purvey in the industry, as end users' ultimate desire is to provide a device with improved electrical performance. As end users strive for better electrical integrity, they continue to pressure substrate manufacturers to improve electrical performance of the substrate. The general desire is for the elimination of the core layer(s) and redesign into what the industry has termed coreless structures. To do this, however, requires very advanced and costly manufacturing techniques at the substrate supplier and also causes great concern at assembly due to lack of rigidity of the substrate, resulting in assembly defects.

Looking to the future, the key issues for substrates and substrate suppliers for next-generation devices will be signal integrity and latency, which will need to be optimized through minimized matched pair routing distances from die to motherboard, surface planarity, cost, and reliability.[5] The laser-embedded technology addresses all of these nicely. Reduced signal path lengths by virtue of feature size reduction, improved planarity by virtue of recessed features, and cost reduction by virtue of layer reduction will ultimately enable these new devices—good news for an industry seeking innovation. □

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