Large area patterning of high density interconnects by novel UV-excimer lithography and photo patternable ORMOCER™-dielectrica

by

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Abstract

The first experiences from Large Area Panel processing (LAP) and Sequential Build Up (SBU) technologies using ANVIK HEXSCAN 2050 SME UV-excimer lithography equipment and photopatternable ORMOCER** dielectrica is presented. The novel equipment enables 5 µm resolution patterning of surfaces up to a size of 610 mm x 610 mm (24 inches x 24 inches). The maximal throughput is up to 27 panels/hour depending on exposure dose requirement. The lightsource is a XeF excimer laser emitting at 351 nm wavelength. The advanced ORMOCER dielectric and optical materials enable low temperature processing also on low cost polymer substrates such as FR-4-epoxy or polymer films. Partitioning between very cheap Standard (lower) Density Interconnect in PCB-substrates and High Density Interconnect (HDI) in the upper thin film layers is possible in order to reduce the number of metal layers and arrive at an optimal performance cost ratio for specific applications. Only one planarizing and metallized ORMOCER layer plus an (ORMOCER) solder mask layer facilitates or enables e.g. flip chip with dense pads on boards. Since lithographic opening of via-holes and lithographic patterning of optical waveguides can be performed simultaneously, the ORMOCER polymer thin film materials technology allows the integration of optical waveguides and high density electrical interconnects with just 3 thin film dielectric/optical layers. Sequential Build Up (SBU) technologies and flexible Large Area Panel (LAP) processing enables: miniaturized low cost & high performance electronics & photonics packaging. Environmentally friendly packaging is possible due to miniaturization, used materials, & processes. Some demonstrator examples from the ongoing European program DONDODEM and other projects are presented.

Keywords

large area UV-excimer lithography, high density interconnect (HDI), sequential build up processing (SBU), FR4-substrate, chip on board, ORMOCER® inorganic-organic photo-polymer, optical waveguide, optical interconnect

**/ ORMOCER is a trademark of Fraunhofer-Institut fuer Silicatforschung, Neunerplatz 2, D-97082 Wuerzburg,Germany

Introduction

The lack of cheap easy-to-industrialize materials, methods, processes and equipment for denser interconnection (HDI) and radio frequency (RF) and optical packaging is a limiting factor for advanced electronic industry. For example; high density interconnect substrates such as Sequentially Build-Up (SBU) multilayer printed circuit boards with microvias and MCM-Ls are becoming increasingly interesting. Companies target e.g.: mobile phones and other portables, but also high value applications such as workstations / servers, mobile and fixed network systems. Relatively few companies are sofar in volume production of "micro-via boards". Materials and technologies of interest for SBU include both laminated films (e.g. Hitachi "BF", DuPont "Vialux") and photopatterned "liquids" (e.g. Ciba "Probelec", Shipley "Multiposit", Hitachi "BL" & "BI", DOW "photo-BCB"and SU-8 from several vendors). Thus there are some photodefinable dielectric materials available on the market that – often under restricted conditions – could be used for MCM and PCB, PWB applications and sequential build up (SBU). A profound new materials development going on trying to meet very broad and advanced demands for both dielectric and optical applications is the development of inorganic-organic polymers, ORMOCERs based on alkoxysilane precursors, see Figure 1 and [1-14].

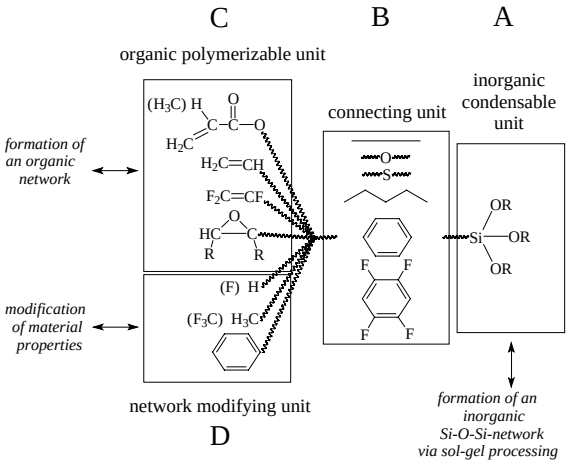

Figure 1 General formula of alkoxysilane precursors for ORMOCER synthesis and their influence on the network and materials properties.

These inorganic-organic hybrid materials offer:
1/ good via-opening and lithographic capabilities
2/ attractive dielectric properties (ε and tan δ),
3/ low processing temperatures (120-180 °C) in contrast to many other thin film materials enabling use of low cost polymeric substrates,
4/ lithograhical patterning to layer heights also above 100 µm which is necessary for most radio frequency applications,
5/ unique photo-embossing possibilities to 2- and 3-dimensional "structures" for microwave, optical and other applications [10, 11, 13],
6/ demonstrated a/ low loss photo patterned optical waveguides superior to all known *(except from waveguides from heavily fluorinated materials which are doubtful from environmental point of view*) and b/ integrated electrical optical packaging expected to become very important in the near future,
7/ compatibility with various metallisation processes,
8/ unique tailorable properties and easy adaptation to all relevant application technologies (spin-on, curtain-coating, printing, dipping etc.),
9/ a very high technical and economical potential to meet a variety of new very advanced demands from e.g. the infocom-, safety-, car-, air-, and space-industry.

In conclusion ORMOCER materials developed by Fraunhofer-Institut fuer Silicatforschung with industrial scale development now performed at Heraeus have unique abilities to combine very good electrical, optical and other properties previously thought not existing in one single material (or material category) alone. They are at the same time offering also an environmentally friendly composition and inherently flame retardant properties and can be processed with both traditional and novel processes such as photo-embossing.

There has also existed a gap in resolution and throughput capability (patterned area/time unit) between processing equipment aimed for chip manufacturing and equipment aimed for e.g. PCB-substrate-manufacturing. This gap has to a large extent been closed by the development of the lithography equipment presented below.

Processing

System overview of UV-lithography equipment

The Anvik HexScan™ 2050 SME lithography system was installed at ACREO AB year 2000. The system is shown in Figure 2. It is designed for the production of high-density microelectronic modules, opto-electronic devices, communication electronics, and displays. The HexScan™ 2050 SME provides the unique capability of imaging large-area panels with high resolution at a high throughput using conventional i-line photoresists. Additionally, with its novel variable-area substrate tiling (VAST™) technology, which enables processing of different multiple-up module configurations, this low-cost system serves both as a volume-production lithography system and as a versatile development tool for prototyping a wide range of products. The modular design of the system also provides equipment upgradeability and choice of user-specified system configurations suitable for different panel sizes and feature resolutions. The key specifications of the Anvik HexScan™ 2050 SME system are shown in Table 1 (see next page).

Figure 2 The Anvik HexScan™ 2050 SME installed at ACREO.

Laser Projection Imaging Technology

In this section, we describe Anviks Laser Projection Imaging technology which delivers large-area exposure capability with high-resolution imaging at high throughput. Figure 3 illustrates Anviks Laser Projection Imaging technology, which is implemented by the combined actions of the scanning stage and the imaging by the projection lens. The substrate and mask are mounted side-by-side on a single

Model 2050 SME System Specifications	
Imaging Technique	Seamless scanning projection
Resolution	5 µm
Projection system	1:1 magnification refractive lenses
Lens image Field Size	30 mm diameter
Depth of Focus	140 µm (in air) 220 µm (in typical dielectric)
Panel Size Capability	610 mm x 610 mm (24 x 24 inches)
Exposure Source	XeF excimer laser (other sources optional)
Exposure wavelength	351 nm (other wavelengths optional)
Overlay Precision	± 1 µm
Alignment system	Automatic
Panel and Mask Handling	Manual with option for automatic
Throughput	27 panels/hour

Table 1 System Specifications

scanning stage that is capable of moving in both X and Y directions. The mask is illuminated from below by a large, hexagon-shaped ultraviolet light beam (30 mm vertex-to-vertex) which is generated by an excimer laser. The pattern on the mask is then transferred to the substrate via a 1:1 magnification projection lens system. The single scanning stage moves (scans) the mask and the substrate in unison along the Y-axis across their respective illumination and imaging regions to traverse the substrate length. The stage then moves along X by an effective scan width, w. The substrate and mask are again scanned along Y as before, after which they are again moved laterally along X, and the process is repeated until the entire substrate is exposed. The complementary overlap between adjacent hexagonal scans produces a seamless and uniform exposure over the whole substrate.

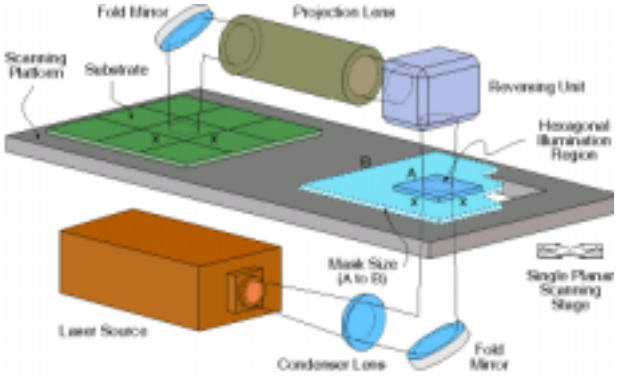

Figure 3 The HexScan™ 2050 SME large-area projection lithography system schematic, showing Anviks seamless scanning technology with variable-area substrate tiling (VAST™).

The seamless scanning technology also provides a platform for the method to populate the substrate with modules of various sizes. The indexing technology of the Variable Area Substrate Tiling (VAST™) Indexing System, enables the user to place multiple patterns of the same or different sizes on one substrate. This technology is achieved by indexing the substrate to different positions with respect to the mask on the scanning platform. As shown in Figure 3, when the substrate is indexed, a selected portion of the substrate is presented to the imaging system for exposure. The Anvik HexScan™ 2050 SME has the capability of tiling modules of any size from 100 x 100 mm (4 x 4 inches) to 300 x 300 mm (12 x 12 inches) over the entire 610 x 610 mm (24 x 24 inch) substrate.

The indexing technology allows the user to pattern modules of various sizes on a single standard substrate, thereby simplifying the handling issues for the rest of the processing steps. Given the micron-level repeatability of the indexing mechanism, it is possible to perform a single, global alignment of the entire mask and substrate and eliminate time spent on site-by-site alignment for some products. Additionally, the technology allows the user to share the processing of several low-volume products on a high-volume platform. Finally, the indexing technology enables the user to employ a mask where the size of the mask is driven by the size of each module. Decreasing mask size makes the manufacturing process more economical and robust.

Thin film Deposition

Deposition of ORMOCERs can be performed with several methods, e.g.: spinning, curtain coating, slit coating, roller coating, screen printing, spray coating and meniscus coating with their various advantages and disadvantages. Spinning is often used to achieve high quality thin films (< 25 µm) . A LAP-spinner from Karl-Suss is available at ACREO also for full sized 610 mm x 610 mm substrates. Large area curtain coating for ORMOCERs have been successfully demonstrated by VIASYSTEMs in their production equipment. Layer thicknesses down to 25 um have been achieved at a substrate speed of about 5 m/sek. With further optimization even thinner layers may be feasible with this low cost production method.

Patterning, development and curing

Patterning of the ORMOCERs is a necessary step both in the fabrication of electrical structures where vias must be opened and in the fabrication of optical structures where e.g. waveguides have to be defined. The lithographic patterning requires a balanced interaction among the prebake, exposure, post-exposure treatment and development (wet etching). The prebake is performed at temperatures between 70 -120 ° C to further drive out the solvent.

The UV-exposure has been performed with the HexScan™ 2050 SME large-area projection lithography system followed by a short post-exposure bake before development takes place. Sofar we have not yet utilized the full-size capability of the equipment in the ORMOCER-work, but rather taking the first steps with smaller substrates, more convenient to work with. Open vias down to 20 µm (or ≈ 2 x film-thickness) have been achieved in 10 µm layers after process optimization.

As can be seen in figure 9 (section with demonstrators) the ORMOCER etching process gives smooth inclined sidewalls resulting in good metal coverage throughout the via and thus low via resistance.

The development can be performed by immersing the thin film object in a tank or by spray or puddle development with a suitable solvent, followed by rinsing in an alcohol and drying in an air or nitrogen stream. Several solvents and solvent combinations can be used, giving a well resolved pattern, normally within seconds.

Final thermal polymerization or post curing has been performed in a convection oven, often at 150 °C overnight.

For the sequential multilayer fabrication, a short intermediate postbake at 150 °C is sufficient for the subsequent metallization process. This process is then repeated to obtain a multilayer structure which is finally polymerized or postcured as described above.

Metallization

Metallization on ORMOCERs can be performed with different methods and metals such as sputtering of aluminum (Al) or copper (Cu) or titanium (Ti, for adhesion, if needed), chemical plating and electroplating of Cu, chemical plating of pad areas with nickel (Ni) and gold (Au) etc. Patterning of metals has been performed using standard resists and wet-chemical methods. Additional details about metallization of ORMOCERs are given in previous publications [e.g. 4 & 5].

Properties of ORMOCERs

Most of the material properties have been presented and discussed previously [1-13] and typical properties will therefore only be summarized briefly here. It should be noted however that new experimental materials with further improved properties are under testing.

Electrical properties:

- permittivity ε at 10 kHz = 3.2
- dielectric loss tan (δ) = 0.006
- volume resistivity $R_D \geq 10^{16}$ Ωcm

Optical properties:

- optical loss α = 0.23 dB/cm at 1310 nm (not fluorinated!)
- refractive index (at 588 nm) = 1.52-1.56 (primary index tuning range).

Temperature stability:

- negligible degradation up to about 300 °C as verified with standard TGA-measurements.

Water-uptake:

- < 0.5 %.

Planarization:

- The degree of planarization (DOP) is very good, ≈ 95 %

HDI-substrate demonstrators

Chip on board

Ericsson has defined and designed electrical test boards to demonstrate high-density low-cost packaging technology for radio base station applications. They have been designed to demonstrate ASIC flip-chip bonding using anisotropically conductive adhesives (ACAs) and for defining design rules for the ORMOCER technology targeted for high density interconnects PCBs.

Compact packaging like flip-chip offers significantly more functionality, smaller size, lighter weight and higher performance at a lower cost. Today, the flip-chip technology is widely used in consumer electronics production. It is currently also being assessed for more high-reliability applications such as telecommunications, industrial electronics and space electronics. Soldering flip-chip technology is the major dominating interconnecting method as it offers reflow capability suitable for mass production. However, for ultra-small pitch flip-chip technology (pitch less than 150 µm), soldering or solder bumping has a clear limit. In this case, flip-chip joining using Anisotropically Conductive Adhesive (ACA) joining may offer a possible "lead-free" environmental friendly solution. ORMOCER technology will facilitate to produce fine conductive lines on PCBs for flip-chip joining processes also due to the excellent planarizing properties. The Degree Of Planarization (DOP) is around 95 % [4].

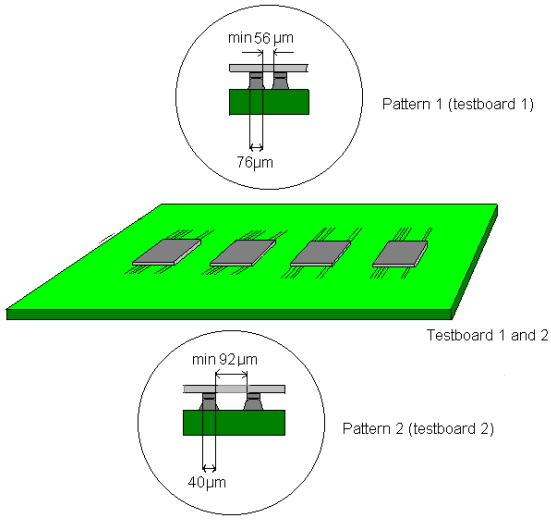

Figure 4 Test Board for ASIC Flip-Chip (FC) Joining Using Anisotropically Conductive Adhesive, size: 100x50 mm, Space/Line: 56/76 µm.

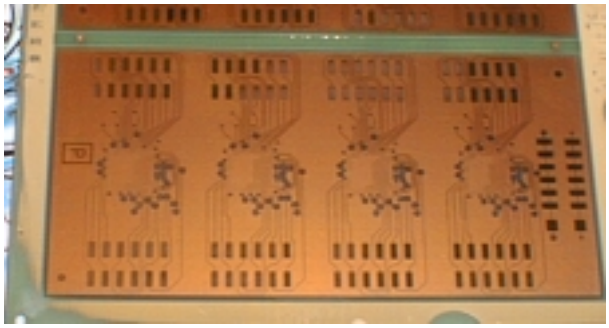

Figure 5 Photograph of (part of) a manufactured FC test board with one ORMOCER-dilectric layer plus metallization (Cu/Ni/Au) on a PCB-substrate with plugged vias. An additional ORMOCER soldering mask layer has been used.

a **b** **c**

Figure 6 Details of test test-board
a: Open FC-soldering area in lower right corner
b: Blind vias, lower major area with ORMOCER solder mask
c: Blind via. Scale-mark = 100 µm

Electrical test vehicle

Using the ORMOCER material supplied by Heraeus and the Anvik lithography equipment, an electrical test vehicle designed by BULL has been manufactured. This one consists of three thin film metal layers (Ti/Cu/Ti, 3µm thick), separated 3 + 1 (upper solder mask layer) 10µm ORMOCER layers, realized on a 150 mm round FR4 board. Several patterns were implemented on it in order to measure electrical properties and to determine achievable design rules in terms of line width, via diameter, registration etc.

Microstrip structures, with different line widths on the two first metal layers over a ground plane implemented on the last PCB layer, have been used to determine the effective

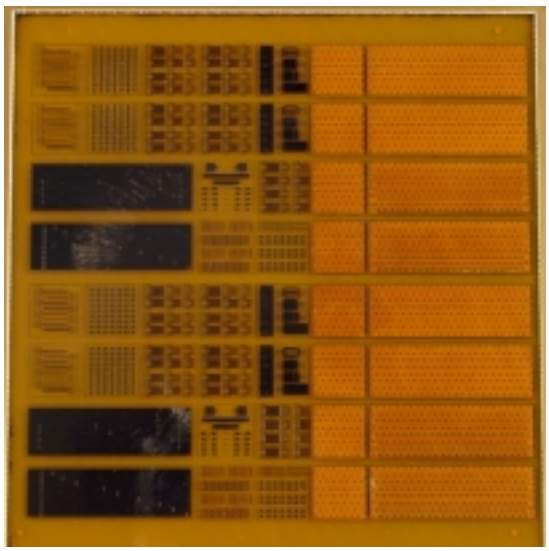

Figure 7 Electrical test vehicle, high density patterns 4 ORMOCER-layers on PCB-substrate.

dielectric constant of the ORMOCER material, ε_r = 3.1, and the characteristic impedances achievable with such line widths (see figure 8).

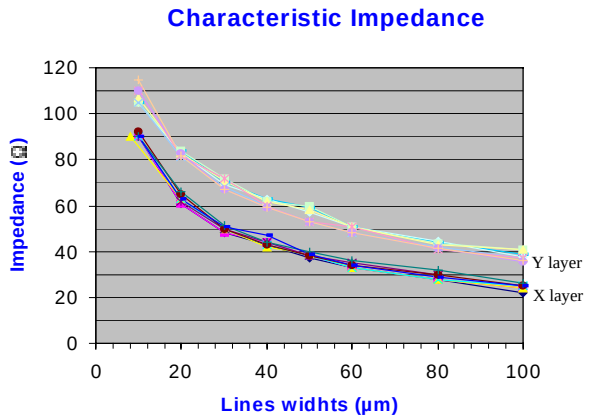

Figure 8 Characteristic impedance versus linewidth in electrical test vehicle.

The X and Y layers represent the two first thin film layers over the ground plane. Measures made on different substrates have shown a good reproducibility of the impedance values. This test vehicle has also proven the feasibility of vias with diameters down to 40 µm (see figure 8).

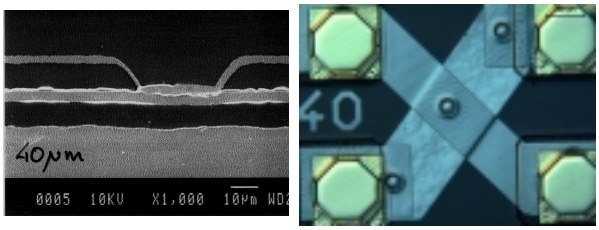

Figure 9
Left: Crossection of 40 µm via in electrical test vehicle.
Right: Top view of 40 µm vias in electrical test vehicle.

O/e-MCM-L/D substrate

A novel concept for a fully integrated opto-electronic package has been presented previously by part of the DONDODEM project consortium [4], figure 10. The unique ORMOCER polymer thin film materials technology allows the integration of optical wave-guides and high density electrical interconnects in just 3 thin film layers.

The substrate used for adding thin film layers is a 4 metal layer (12 µm Cu) PCB with microvia-technology with BGA-pads underneath eliminating the need of any extra package for connection to next packaging level. On top of the substrate three ORMOCER dielectric layers have been deposited and UV-patterned. Each ORMOCER layer has sputtered aluminum (3 µm) on top. The pad areas have additional aluminum (3µm), titanium (0.1 µm), copper (0.4 µm), nickel (3 µm) and on top gold (0.2 µm) for bonding of the components. The three ORMOCER thin film layers incorporate both high density electrical interconnects, as in MCM-D-technology, and also optical waveguides. The middle (second) dielectric layer (20 µm thick) is partially used for the multi mode waveguides (core) and has therefore a higher refractive index (Δn≈0.020) than the first and third dielectric layers (each 10 µm thick). The first and third dielectric layers are also used as cladding layers for the waveguides. All dielectric layers have electrical vias. A thin (3 µm) ORMOCER passivation layer finishes the layer buildup.

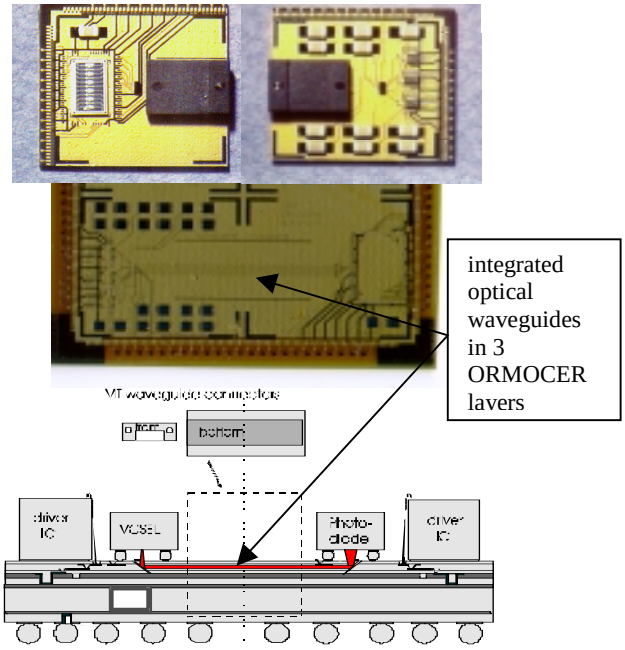

Figure 10 O/e-MCM-L/D demonstrator [4] with 3 ORMOCER-layers incorporating both electrical interconnects and optical waveguides (waveguides seen as ”weak” horizontal straight lines in the middle of the photograph). Bottom part showing cross-section with optical waveguides in the second ORMOCER layer.

The new lithography equipment in combination with the unique possibility for simultaneous use of the ORMOCERs as dielectrica materials and optical waveguide/cladding materials enables new opportunities for rational production of printed circuit boards and backplanes with both high density electrical interconnects and optical interconnects. Multimode waveguides, typically 50 µm wide can easily be patterned whereas singlemode waveguides in most cases probably need higher resolution than the lithography equipment can provide today. Also advanced electro-optical module substrates can be rationally produced to low cost due to the high throughput of up to 27 x 61 x 61 ≈ 100 000 cm^2 area of patterned panel per hour, i.e. corresponding to e.g. a maximum of ≈ 10 000 ”cm-sized” modules per hour if each module has been processed with 5-10 lithographic steps.

Conclusions

A concept considered to have a great potential for achieving *low cost & high performance electronics & photonics packaging* have been proposed and comprises:

- Photo patternable ORMOCER™-dielectrica materials with simultaneosly good dielectric, optical, thermal, planarizing and low temperature processing (120 - 180 °C) properties,

- The ANVIK HexScan™ 2050 SME lithography equipment providing the unique capability of imaging large-area panels (up to 610 mm x 610 mm) with high resolution (5 µm) at a high throughput (up to 27 panels/ hour) using conventional i-line sensitive resists and photopatternable dielectrica,

- The overall flexibility of the whole process- and packaging concept allows e.g.:
  1. integrated electrical and optical packaging,
  2. optimized partitioning between base-substrate with standard PCB *low density interconnects* and added thin films with *high density interconnects*,
  3. to place multiple patterns of the same or different sizes on one substrate,
  4. to share the processing of several low-volume products on a high-volume platform.

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References

1. M. Popall, J.Kappel, M. Pilz and J. Schulz, *"New patternable materials for Electronic packaging"*,Mat. Res. Soc., Symp. Proc. **264**, 353-359 (1992)
2. A. Dabek, M. Popall, B. Olsowski, Ch. Kallmeyer and H. Reichl, "Evaluation of ORMOCER's for microelectronics applications", *Proc. 12th European Microelectronics Conference*, Venice, Italy, May 1997, pp 125-32
3. M. Popall, A. Dabek, M. E. Robertsson, G. Gustafsson, O.-J. Hagel, B. Olsowski, R. Buestrich, L. Cergel, M. Lebby, P. Kiely, J. Joly, D. Lambert, M. Schaub and H. Reichl, *"ORMOCER's - New, photo-patternable dielectric and optical materials for MCM-packaging"*, at 48th Electronic Components and Technology Conference (ECTC'98), May 26-28, 1998 Seattle, USA
4. M. E. Robertsson, O.-J. Hagel, G. Gustafsson, A.Dabek, M. Popall, L. Cergel, P. Wennekers, P. Kiely , M. Lebby and T. Lindahl, *"O/e-MCM-packaging with new patternable dielectric and optical materials"*, at 48th Electronic Components and Technology Conference (ECTC'98), May 26-28, 1998 Seattle, USA
5. M. Popall, A. Dabek, M.E. Robertsson, S. Valizadeh, O.J. Hagel, R. Buestrich, R. Nagel , L. Cergel, D. Lambert, M. Schaub, *„ORMOCER s - Inorganic-organic Hybrid Materials for e/o-Interconnection-Technology"*, proceedings of Fifth International Conference on Frontiers of Polymers and Advanced Materials, 21.- 25. Juni 99, Poznan, Polen, MOLECULAR CRYSTALS & LIQUID CRYSTALS, in print.
6. M. Popall, R. Buestrich, F. Kahlenberg, A. Andersson, J. Haglund, M. E. Robertsson, G. Blau, M. Gale, O. Rösch, A. Dabek, J. Neumann-Rodekirch, L. Cergel and D. Lambert: *"Electrical and optical Interconnection-Technology Based on ORMOCER - Inorganic-organic Hybrid Materials"*, MRS 2000 Spring-Meeting San Francisco 24. – 29. April 2000, Mater. Res. Soc. Proc. Symposium Proceeding, in print.
7. R. Buestrich, F. Kahlenberg, M. Popall*, A. Martin, O. Rösch: *"Low Si-OH ORMOCER®s for Dielectrical and Optical Interconnection Technology"*, MRS 2000 Spring-Meeting San Francisco 24. – 29. April 2000, Mater. Res. Soc. Proc. Symposium Proceeding in print.
8. R. Müller-Fiedler, J. Graf. O. Rösch, S. Hiemer, L. Fröhlich, R. Büstrich, T. Stolle, *" Inorganic-Organic Functional Polymers for Multilayer Microwave Circuits"*, Materials Week, 25-28.9.2000
9. M. Robertsson, G Gustafsson, O-J Hagel, A Dabek and M Popall, *"New Patternable Dielectric and Optical Materials for MCM-L/D- and o/e-MCM-packaging"*, The first International Conference on Polymers in Electronic packaging (PEP´97), Norrköping, Sweden, October 26-30, 1997
10. D Schönfeldt, O. Rösch, P. Dannberg, A. Bräuer, R. Muller-Fiedler, M. Popall, R. Buestrich, *"Enhanced Performance of Polymer waveguides by Replication and UV-patterning in ORMOCER"*, SPIE, Proc. Vol. 3135, 1997, pp 53-63.
11. P. Dannberg, R. Bierbaum, L. Erdmann, A. Krehl, E.B. Kley, A. Braeuer, *„Microoptical elements and their integration to glass and optoelectronic wafers"* Microsystem Technologies 6 (1999) 41-47
12. O. Roesch, W. Bernhard, R. Mueller-Fiedler, P. Dannberg, A. Braeuer, R. Buestrich, M. Popall, *„High performance low cost fabrication method for integrated polymer optical devices" Organic Photorefractives, Photoreceptors, Waveguides, and Fibers* in Proceedings SPIE vol. 3799, p. 214-224, Bellingham 1999
13. G. Blau, M. T. Gale, J. Söchtig, Ch. Zschokke, R. Hövel and K. Gulden, *'Tunable VCSEL with integrated heater and planar waveguide wavelength monitor'*, Proc. Optical MEMS 2000, Kauai, 27-31 August 2000.
14. U Steppel, P. Dannberg, C. Wächter, A. Bräuer and P. Nicole: *"A novel manufacturing technology for stacked polymer waveguide devices"*, (European Conference on Integrated Optics, ECIO, April 2001 Paderborn, Germany), proceedings to be published
15. K. Jain et al., *"Large-Area, High-Throughput, High-Resolution Lithography Systems for Flat-Panel Displays and Microelectronic Modules"*, Proc. SPIE, Vol. 3331, p. 197, 1998.